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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,938	10/13/2006	Peter J. Geiss	BUR920030152US2	6841

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IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
12/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,938	GEISS ET AL.	
	Examiner	Art Unit	
	SCOTT R. WILSON	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,16,18-21,24-27,30 and 31* is/are rejected.

7)☒ Claim(s) *17,22,23,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/13/06, 8/16/07, 10/22/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15, 16 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato (US 5,986,326). As to claim 15, Kato, Figures 11 and 12, discloses a method of making a transistor, said method comprising: forming a extrinsic base (5) above an intrinsic base (4); protecting a portion of said extrinsic base using a sacrificial mask that is positioned over a center of said extrinsic base; siliciding exposed portions of said extrinsic base, wherein said siliciding process leaves a non-silicided portion over said center of said extrinsic base (best seen by comparing the silicide layer (7') between Figures 11 and 12); forming an emitter opening (18) through a center of said non-silicided portion of said extrinsic base; forming spacers (13) in said emitter opening; and forming an emitter (6), with emitter contact (16), in said emitter opening, wherein said spacers separate said emitter from silicided portions of said extrinsic base.

As to claim 16, Kato, Figure 11, discloses before forming said extrinsic base: patterning an insulator (6) over said center of said intrinsic base (4); and epitaxially growing said extrinsic base (5) over said insulator and said intrinsic base.

As to claim 18, Kato, Figure 11, discloses that said spacers (13) are formed on said insulator (6).

As to claim 19, Kato, Figure 11, discloses that said siliciding process forms said silicided portions (7') of said extrinsic base horizontally adjacent to said non-silicided portion.

As to claim 20, Kato, Figure 9E, discloses before forming said emitter opening, forming an insulator layer (3) above said extrinsic base, wherein said emitter opening is formed through said insulator layer (Figure 9F).

Claims 21 and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato. As to claim 21, Kato, Figure 11, discloses a method of making a transistor, said method comprising: forming a lower semiconductor structure (2) having a first-type impurity; forming a middle semiconductor region (4) above said lower semiconductor structure, said middle semiconductor region having a second-type impurity complementary to said first-type impurity; protecting a portion of said middle semiconductor region using a sacrificial mask that is positioned over a center of said middle semiconductor region; siliciding exposed portions of said middle semiconductor region, wherein said siliciding process leaves a non-silicided portion over said center of said middle semiconductor region (best seen by comparing silicided layer (7') between Figures 11 and 12); forming an upper semiconductor structure opening (18) through a center of said non-silicided portion of said middle semiconductor region; forming spacers (13) in said upper semiconductor structure opening; and forming an upper semiconductor structure (15) and (16) in said upper semiconductor structure opening, wherein said spacers separate said upper semiconductor structure from silicided portions of said middle semiconductor region.

As to claim 24, Kato, Figure 11, discloses that said spacers (13) are formed on said insulator (6).

As to claim 25, Kato, Figure 11, discloses that said siliciding process forms said silicided portions (7') of said extrinsic base horizontally adjacent to said non-silicided portion.

As to claim 26, Kato, Figure 9E, discloses before forming said upper semiconductor structure opening, forming an insulator layer (3) above said middle semiconductor region, wherein said upper semiconductor structure opening is formed through said insulator layer (Figure 9F).

Claims 27, 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato. As to claim 27, Kato, Figure 11, discloses a method of making a bipolar complementary metal oxide semiconductor (BiCMOS) device, said method comprising: forming a collector (2); forming shallow trench isolation regions (3) adjacent said collector; forming an intrinsic base (4) above said collector; forming a raised extrinsic base (5) above said intrinsic base; protecting a portion of said extrinsic base using a sacrificial mask that is positioned over a center of said extrinsic base; siliciding exposed portions of said extrinsic base, wherein said siliciding process leaves a non-silicided portion over said center of said extrinsic base (best seen by comparing silicided layer (7') between Figures 11 and 12); forming an emitter

opening (18) through a center of said non-silicided portion of said extrinsic base; forming spacers (13) in said emitter opening; and forming an emitter (6) in said emitter opening, wherein said spacers separate said emitter from silicided portions of said extrinsic base.

As to claim 30, Kato, Figure 11, discloses that said siliciding process forms said silicided portions (7') of said extrinsic base horizontally adjacent to said non-silicided portion.

As to claim 31, Kato, Figure 11, discloses that said spacers (13) are formed on said insulator (6).

Allowable Subject Matter

Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where said process of epitaxially growing said extrinsic base *grows polysilicon above said insulator and single crystal silicon above the exposed portions of said intrinsic base*.

Claims 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where, before forming said middle semiconductor region: forming a *silicon layer over said lower semiconductor regions*; patterning an insulator over said center of said silicon layer; and epitaxially growing said middle semiconductor region over said insulator and said silicon layer.

Claims 28 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed method where, before forming said extrinsic base: patterning an insulator over said center of said intrinsic base; and *epitaxially growing said extrinsic base over said insulator* and said intrinsic base.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
December 25, 2008

/Evan Pert/

Primary Examiner, Art Unit 2826